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UTILITY PATENT APPLICATION TRANSMITTAL LETTER UNDER 37 C.F.R. 1.53(b)	ATTORNEY DOCKET NO.: 10191/955

Address to:
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Washington D.C. 20231
Box Patent Application

Transmitted herewith for filing is a patent application.

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For: **METHOD OF PRODUCING STRUCTURED WAFERS**

1. Enclosed are:
   - [X] 2 sheet(s) of drawing(s).
   - [ ] An Assignment of the invention and an accompanying Assignment Recordal.
   - [X] A certified copy of German Patent Application No. 1 98 03 186.6-33 filed on January 28, 1998, on which the claim to priority is based.
   - [X] A declaration/power of attorney (unsigned).
   - [ ] An Information Disclosure Statement along with an accompanying PTO-1449 form.
   - [ ] Other:_____

2. The filing fee has been calculated as shown below:

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TOTAL CLAIMS	9 - 20 =	0	18.00	0.00
INDEPENDENT CLAIMS	1 - 3 =	0	78.00	0.00
MULTIPLE DEPENDENT CLAIM PRESENT			260.00	0
*Number extra must be zero or larger			TOTAL	760.00
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5. A duplicate copy of this letter is enclosed for that purpose.

Respectfully submitted,

Dated: 1/27/98

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METHOD OF PRODUCING STRUCTURED WAFERS

Background Information

Wet chemical etching methods of structuring wafers are already known. A photoresist method is generally used to define a structure. Increasing quality demands in production of integrated circuits and micromechanical sensor arrangements require removal of the photoresist from the wafers used, because otherwise residues of resist will be entrained throughout the various process steps in conveyance of the wafers. However, after the resist has been removed from the edge of the wafer, it is unprotected when exposed to etchant media.

Summary Of The Invention

The method according to the present invention has the advantage that passivation of the wafer edge is guaranteed despite removal of the resist there without having to use etching boxes, for example, to protect the wafer edge from the aggressive etchant medium. By combining wafer edge passivation as a negative process with the positive process of determining the areas to be etched subsequently, a method is provided which is inexpensive and nevertheless meets high quality demands. The wafer edge remains protected from etchant media without photoresist at the edge and without the use of etching boxes.

By removing a nitride layer only in subareas and then applying a thin passivation layer in the subareas, two or more step etching processes can also be carried out while preserving the wafer edge passivation.

It is especially advantageous to use an oxide layer as a passivation layer, which is applied in a LOCOS process (LOCOS = "local oxidation of silicon").

Brief Description Of The Drawings

Figure 1 shows a first embodiment of the method according to the present invention.

Figure 2 shows a second embodiment of the method according to the present invention.

Detailed Description

Figure 1 shows a first embodiment of the method according to the present invention as a two-sided one-step etching process. Part 1 shows a cross-sectional view of wafer 20 with a front side 22, a back side 23 and an edge area 21. The wafer is shown only partially, continuing toward the left, where it is delimited by another edge area (not shown). A nitride layer is applied to the wafer by gas phase deposition. Then the nitride layer is structured by a conventional photoresist technique, with the resist being applied to the nitride layer, exposed selectively and then developed; (when using a positive resist) the exposed part of the resist is next removed, then the exposed part of the nitride layer is removed, usually by a plasma etching process, and finally the remaining unexposed part of the resist is removed, e.g., by ashing the resist in an oxygen plasma. Nitride structuring is performed first on the front side of the wafer, as shown in Part 1; this structuring yields structured nitride layer 25. Unstructured nitride layer 24 is still imaged on the back side.

In another step, the nitride layer on the back side of the wafer is structured similarly; accordingly, Part 2 shows structured nitride layer 26 on the back side as the result of this nitride structuring. A passivation layer is applied in another step shown in Part 3. This embodiment shows an oxide layer 27 used as a passivation layer produced by selective growth in a thermal process, a LOCOS process, at about 1100°C. In another step, the nitride layer is removed selectively with regard to the oxide by a plasma etching process or by etching in hot phosphoric acid. The result is shown in Part 4: a wafer 20 with a structured oxide layer, with the oxide layer also completely surrounding wafer edge 21. In another step the silicon is etched by an anisotropic etching process, e.g., in a KOH bath. The etching process is performed until reaching the desired etching depth or until desired through hole 29 has been etched out. In another step the passivation layer is removed, e.g., by applying an etchant medium containing

hydrofluoric acid. Part 5 shows the result of the etching step and removal of the passivation. Structured wafer 30, which is shown in cross section, has a through hole 29 and a cavern area 28.

Figure 2 shows another embodiment of the method according to the present invention. First the procedure described in Parts 1 through 3 of Figure 1 is followed. In another step, however, the nitride layer is removed in a subarea 40 of the positive area of the surface of the wafer. The positive area is formed by the part of the surface of the wafer covered with the nitride layer. Then a photoresist method is used in the usual manner to obtain a structure like that shown in Part 6. Wafer 20 has a structured nitride layer 25 on the front side and a structured nitride layer 26 on the back side. The remainder of the surface of the wafer is covered with an oxide layer except for subregion 40. Then an oxide layer 41 is applied in subregion 40 in a second local oxidation (thermal oxidation process, LOCOS process). Here again, as in the first local oxidation, selectivity for the areas covered with a nitride layer is guaranteed. Part 7 shows the result of this process step: a wafer provided with a thin oxide layer 41 in subregion 40 and either a thick oxide layer or a nitride layer in other areas. In another step, the nitride is completely removed selectively with respect to the oxide in a plasma etching process.

The wafer with the structure illustrated in Part 8 is then exposed to a wet chemical etching process in a KOH bath. First the wafer is pre-etched in the area of through hole 29 to be formed later, in order to partially remove the silicon and produce recesses 42 on both sides (see Part 9). Then thin oxide layer 41 is removed in subregion 40 with a hydrofluoric acid etchant medium which attacks all areas of the silicon dioxide layer in the immersion bath; however, since the oxide layer in subregion 40 is thinner than the remaining layer, it can be removed completely selectively with respect to the remaining oxide layer in subregion 40 if the etching process with the hydrofluoric acid etchant medium is terminated as soon as thin oxide layer 41 is removed (Part 10). Finally, the wafer is etched in KOH until the silicon is removed to the final etching depths.

Part 11 shows the structured wafer after subsequent removal of the passivation layer; it has a through hole 29 and a shallow cavern 43. A structuring of the wafer has been achieved through the procedure of a two-sided two-step KOH etching process illustrated in Figure 2 in comparison with Figure 1, resulting in a cavern 43 which is shallower than cavern 28 from Figure 1.

Other structures with KOH etching of the front and/or back side in a one- or two-step KOH etching process can be derived easily from the embodiments shown in Figures 1 and 2. Of course, it is also possible to derive multi-step etching processes where more than two different oxide thicknesses are implemented to permit multiple gradations in the final etching depths. Important in all embodiments is the production of wafer passivation in a photoresist technique in a type of negative process where the resist has been removed in a preceding structuring operation, i.e., at the edge. In the embodiments, the positive areas are to be understood as the areas of the wafer surface covered with a nitride layer. The other areas of the surface of the wafer are negative areas, also including edge areas of the wafer, i.e., precisely the areas where passivation is to be guaranteed.

The standard IC photoresist technique with the usual removal of resist from the edges before exposure can be used as the photoresist technique. As an alternative, it is also possible to use photoresist methods where the resist is not removed from the edge of the wafer until after exposure of the photoresist or after exposure and developing of the photoresist.

What Is Claimed Is:

1. A method of producing a micromechanical sensor arrangement, comprising the steps of:

providing a wafer having a surface and edge areas;

dividing the surface of the wafer into positive areas, to be subsequently etched in a wet chemical etching process, and negative areas including the edge areas of the wafer;

providing the negative areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process;

etching the wafer in the wet chemical etching process; and

removing the passivation layer.

2. The method according to claim 1, wherein the dividing step includes the sub-steps of:

applying a nitride layer; and

structuring the nitride layer using a photoresist technique so that the positive areas are defined by a part of the surface covered with the nitride layer.

3. The method according to claim 2, further comprising the step of removing the nitride layer at least in subareas of the positive areas, after the negative areas are provided and before the wafer is etched.

4. The method according to claim 3, further comprising the steps of:

applying a thin further passivation layer in the subareas, after the removal of the nitride layer in the subareas and before the wafer is etched; and

completely removing the nitride layer.

5. The method according to claim 2, wherein the photoresist technique is an integrated circuit photoresist technique.

6. The method according to claim 2, wherein the structuring step includes

the step of removing a photoresist at an edge after exposing the photoresist.

7. The method according to claim 6, wherein the photoresist is removed after exposing and developing the photoresist.

8. The method according to claim 1, wherein the passivation layer is an oxide layer.

9. The method according to claim 8, further comprising the step of applying the oxide layer in a LOCOS process.

Abstract Of The Disclosure

A method of producing structured wafers guarantees that the edge of the wafer will be protected from attack by an aggressive etchant medium without applying a photoresist to the edge and without using additional mechanical measures. In a type of negative process, a passivation layer is applied to the areas that are not to be structured, including the edge area of the wafer.

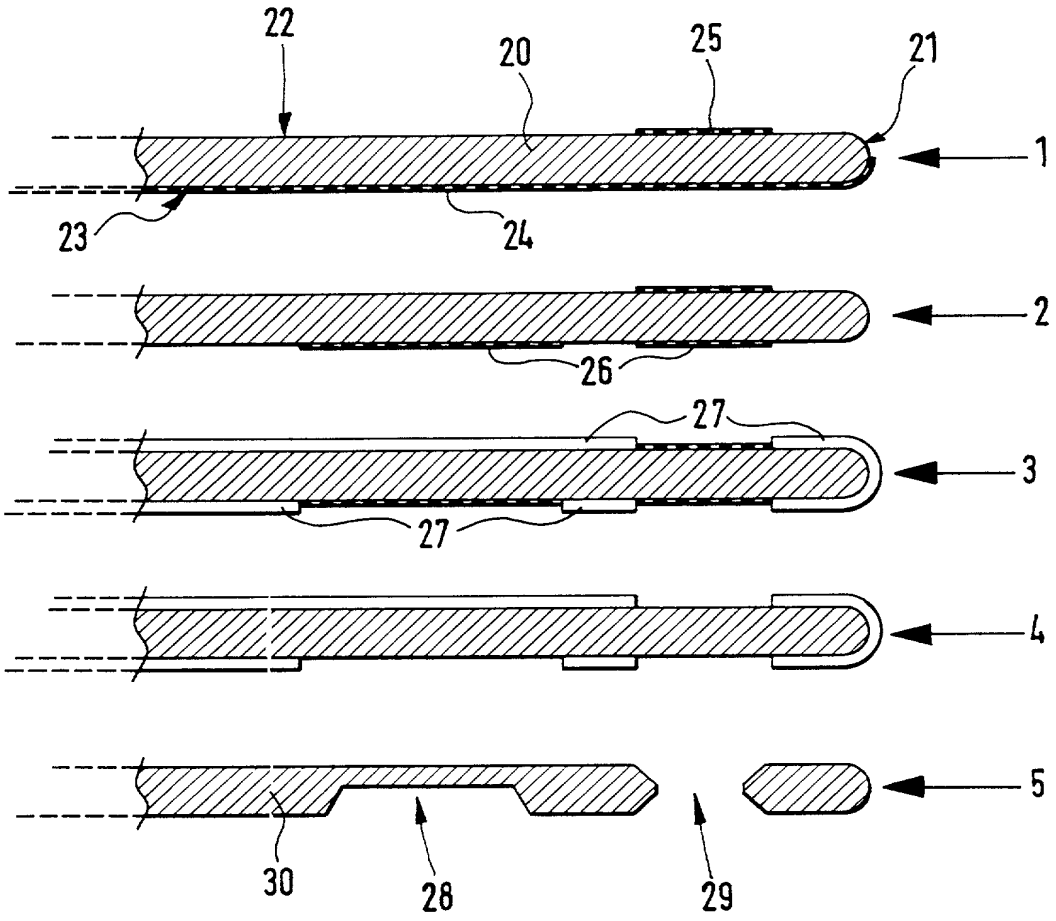

Fig. 1

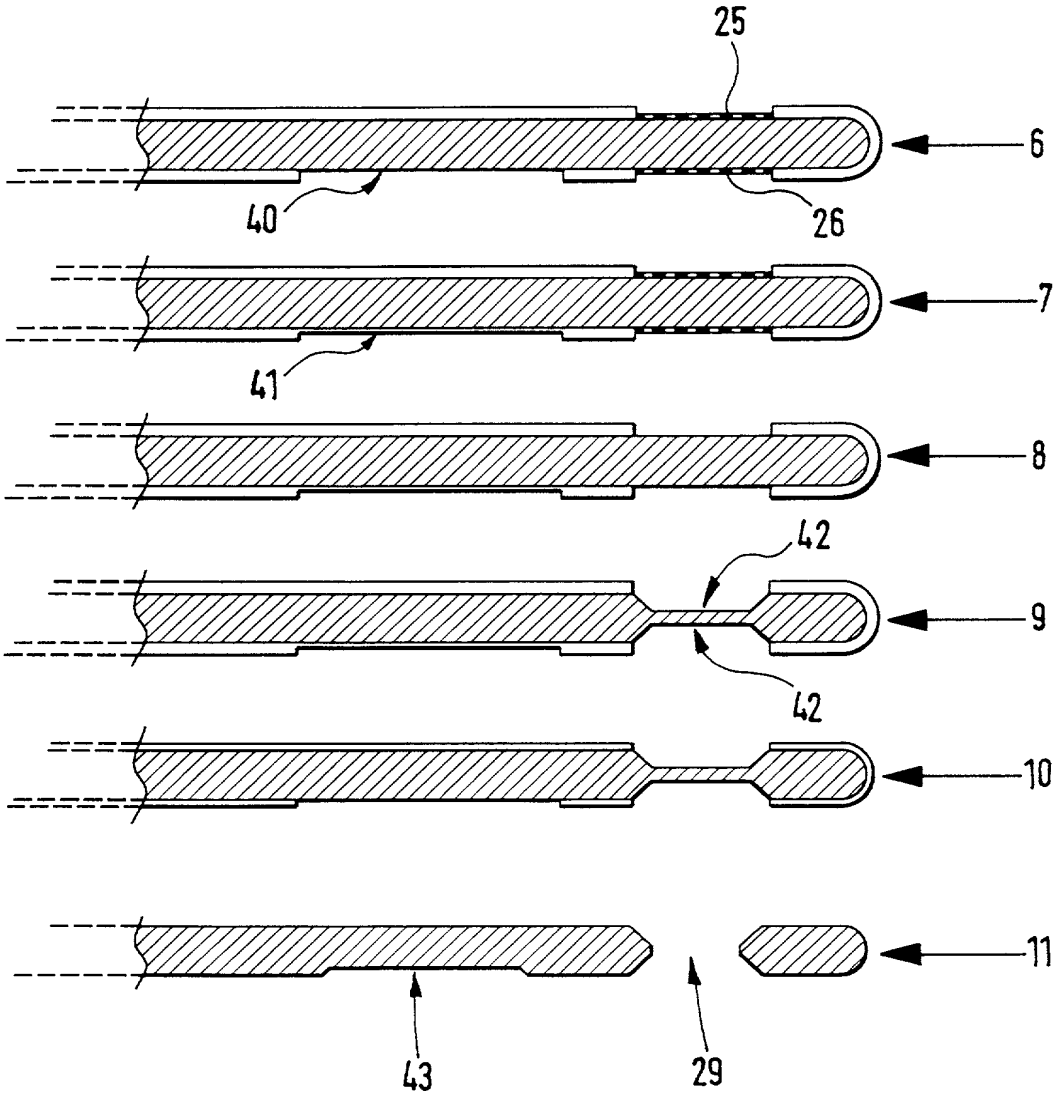

Fig. 2

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COMBINED DECLARATION AND
POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD OF PRODUCING STRUCTURED WAFERS**, and the specification of which:

[X] is attached hereto;

[ ] was filed as United States Application Serial No. _____ on _____, 19__ and was amended by the Preliminary Amendment filed on _____, 19__.

[ ] was filed as PCT International Application Number _____ on the _____ day of June, 19__.

[ ] an English translation of which is filed herewith.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international applications(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

EL799488961US

PRIOR FOREIGN/PCT APPLICATION(S)
AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

Country : Germany

Application No. : 1 98 03 186.6-33

Date of Filing: January 28, 1998

Priority Claimed
Under 35 U.S.C. § 119 : [X] Yes [ ] No

I hereby claim the benefit under Title 35, United States Code § 120 of any United States Application or PCT International Application designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR
PCT INTERNATIONAL APPLICATIONS
DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120

U.S. APPLICATIONS

Number :

Filing Date :

PCT APPLICATIONS
DESIGNATING THE U.S.

PCT Number :

PCT Filing Date :

I hereby appoint the following attorney(s) and/or agents to prosecute the above-identified application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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